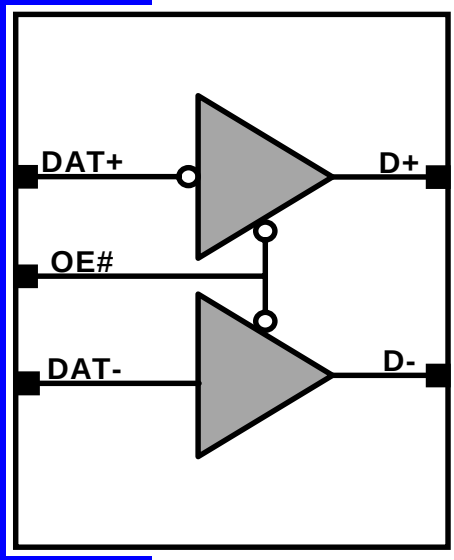
DESIGN GUIDE FOR A LOW SPEED BUFFER FOR THE UNIVERSAL SERIAL BUS



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The information in this document is subject to change.

Table Of Contents

1. INTRODUCTION

This paper will describe a CMOS output buffer that is suitable for use as a Universal Serial Bus (USB) low speed buffer. It uses capacitor feedback to control the edge rates to meet the 75 ns minimum and 300 ns maximum rise and fall times. It should be easily realizable in any standard CMOS process. A design example for a 0.8 μm process is given at the end of this paper.

This design assumes the reader is fully aware of the USB specification and understands something of analog circuits such as current mirrors, cascodes and differential amplifiers. Those unfamiliar with analog design concepts can find information about them in the references in the bibliography at the end of the paper.

2. BASIC LOW SPEED BUFFER

2.1 Elements of the Basic Buffer

Figure 2-1 shows the basic USB low speed buffer block diagram.

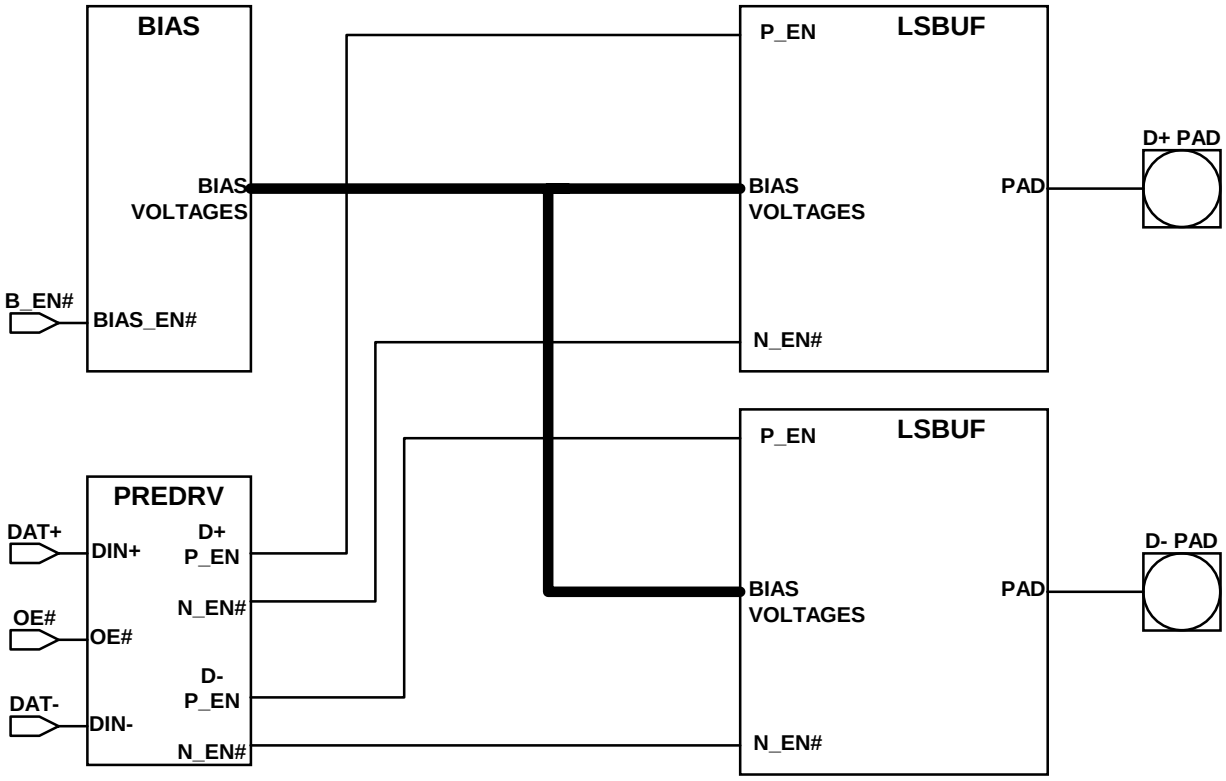


Figure 2-1 - Basic USB low speed buffer block diagram

There are three cells in the buffer design: PREDRV, LSBUF and BIAS.

PREDRV is the predriver cell that controls when the buffer is driven to its differential zero, differential one, single-ended zero or to its high impedance state. It is made up of standard logic gates. The outputs of PREDRV affect the pad states as shown in Table 1.

Table 1 - PREDRV control output truth table

D+	D-	OE#	D+ LSBUF			D- LSBUF			Pad State
			P_EN	N_EN#	D+ PAD	P_EN	N_EN#	D- PAD	
X	X	1	0	1	Z	0	1	Z	High imped.
0	1	0	0	0	0	1	1	1	J-State (Diff. zero)
1	0	0	1	1	1	0	0	0	K-State (Diff. one)
0	0	0	0	0	0	0	0	0	Single-ended zero

LSBUF drives the pad with controlled rise and fall times. The basic circuit elements for LSBUF are shown in Figure 2-2. The connections for the other cells and pad are also shown. The details of this circuit are covered in the next section.

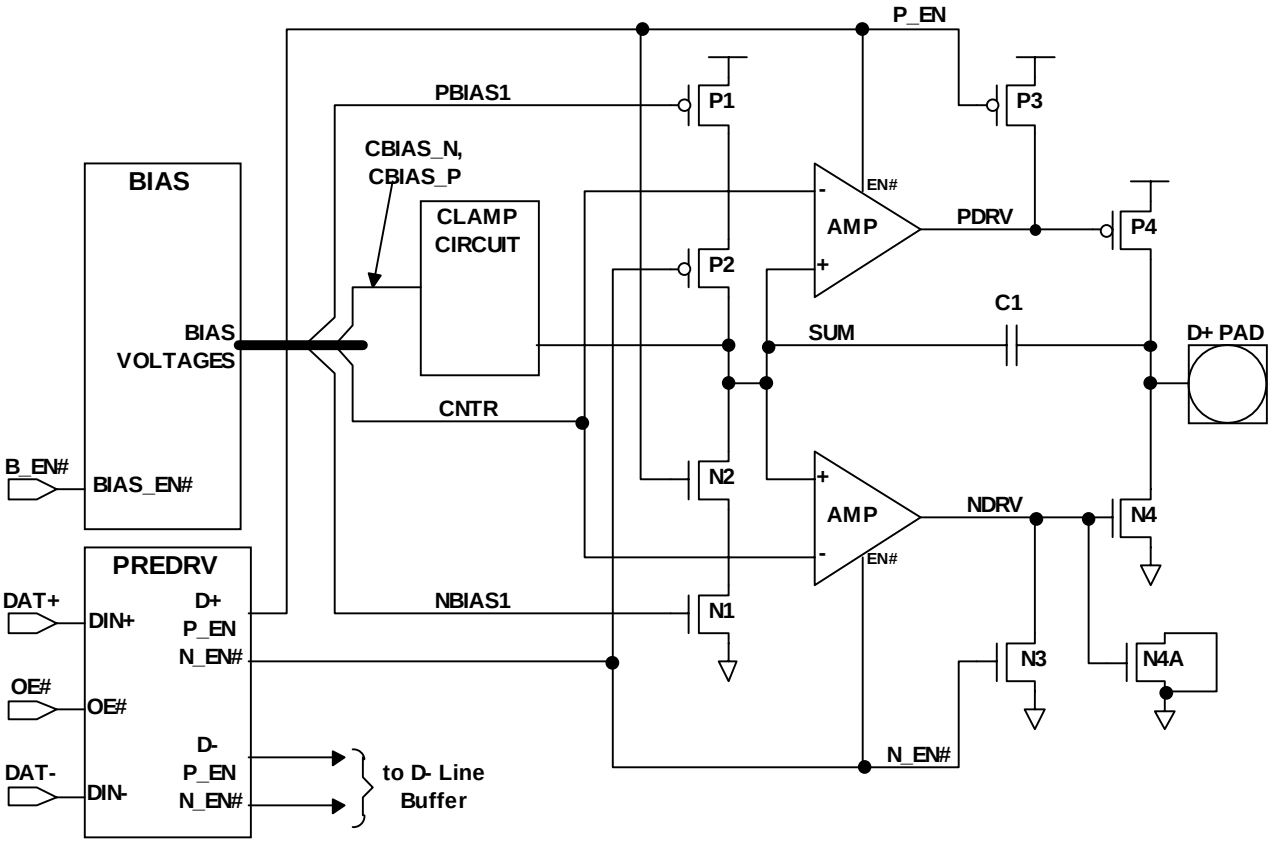


Figure 2-2 - LSBUF Circuit (with connections to BIAS and PREDRV)

The **BIAS** cell is shown in Figure 2-3 provides the control voltages for the LSBUF cells. PBIAS1 and NBIAS1 control current mirrors in LSBUF that determine the buffer edge rate. The current through the resistors sets the current level. PBIAS2 and NBIAS2 are used to bias these current mirrors and some current steering circuits in LSBUF. CNTR sets the DC bias point of the SUM node in LSBUF along with clamp bias voltages CBIAS_N and CBIAS_P. The clamp circuit in LSBUF is explained below. The BIAS_EN# input enables the BIAS cell when low and powers the circuit down when high.

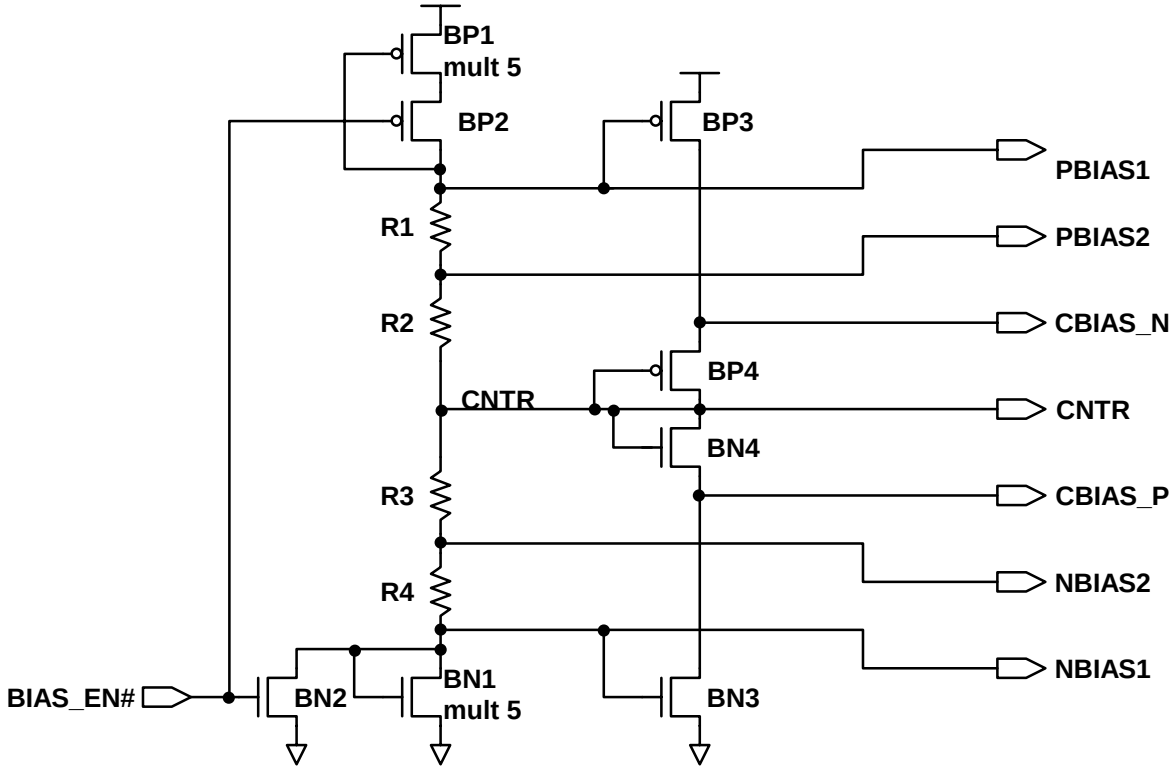


Figure 2-3 - BIAS cell circuit

2.2 Theory of Operation

2.2.1 A SIMPLIFIED MODEL

At the heart of the LSBUF buffer design is an integrator. Each buffer output driver transistor has an amplifier with capacitor feedback and a current source to force a linear ramp on the buffer's output. The amplifier and current source that controls a buffer's fall time (through the N4 pull-down transistor) is shown in abstracted block form in Figure 2-4. A virtual ground is established on the node SUM at Vcc/2. The node SUM is held close to Vcc/2 at all times by bias circuits not shown. Also, when the buffer is active during a transition, the feedback on the amplifier will act to keep SUM close to the virtual ground.

The falling edge rate is controlled by the circuit of Figure 2-4 as follows: The edge rate of the pad determines the current flow (i_{CAP}) through capacitor C1. At the proper edge rate, i_{SRC} is set to be equal to i_{CAP} (i_{IN} is zero). If the rate is too slow, then i_{CAP} is less than i_{SRC} and SUM is pulled above Vcc/2. This makes the amplifier drive its output higher, which increases the gate drive on output transistor N4, increasing its strength and increasing the edge rate. The edge rate is increased until i_{CAP} equals i_{SRC}. Conversely, if the rate is too fast, then i_{CAP} is greater than i_{SRC} and SUM is pulled below Vcc/2. This makes the amplifier drive its output lower, which decreases the gate drive on output transistor N4 and decreases the edge rate.

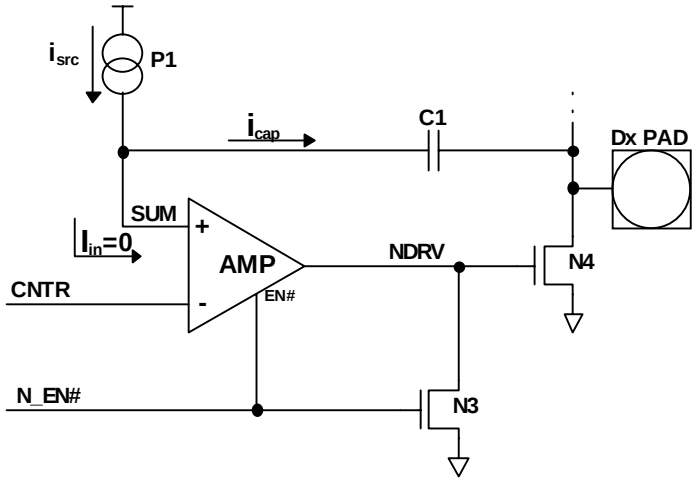


Figure 2-4 - Simplified circuit for pull-down edge rate control

The current through the feedback capacitor C1 current (i_{CAP}) is set by the edge rate (slope) of the output pad by:

$$i_{CAP} = C1 \cdot \frac{dv}{dt} \qquad [1]$$

The voltage on SUM does not move much, so the dv/dt across the capacitor is the rate of change (slope) of the output voltage. If i_{IN} is not zero (i.e.: if some bias current is required by the amplifier), the above description is modified only in that i_{SRC} is increased by the value i_{IN} and the node SUM is charged or discharged based on the sign of (i_{SRC} - i_{CAP} - i_{IN}).

2.2.2 DERIVATION OF THE UNIT CURRENT

The value of i_{CAP} is set by the target slope and the value of C1. The USB specification for a low speed buffer's rise and fall times is 75 ns (min.) to 300 ns (max.). This design example will take a target value of 150 ns, geometrically half way between the minimum and maximum values. The value of C1 is limited by the capacitors available in standard logic CMOS technologies. Device gate capacitance is the highest per square, but is not very suitable because of the large voltage coefficients and large parasitic elements. A reasonable capacitor can be made with a poly-metal1-metal2 sandwich. It is practical to make a capacitor up to 1 pF by this means. The slope (dv/dt) of the output is set by the rise/fall time between 10% and 90% of the output waveform. The maximum swing is 3.6 volts which yields a 10-90 swing of 3.0 volts or a slope of 20 V/µs. Using a slope of 20 V/µs, a 1 pF feedback capacitor and equation [1]:

$$i_{CAP} = C1 \cdot \frac{dv}{dt} = 1.0\,pF \cdot \frac{3\,V}{150\,ns} = 1.0\,pF \cdot 20\,\frac{V}{\mu s} = 20\,\mu A$$

The 20 µA current will be used in several ways and is the basic unit of current in this buffer design. Therefore, the i_{CAP} of 20 µA will be designated the "**unit current**."

2.2.3 BASIC BUFFER OPERATION

Figure 2-5 shows the portion of the buffer outlined in Figure 2-4 expanded to equivalent transistors. (The clamping circuit for the SUM node is not shown.)

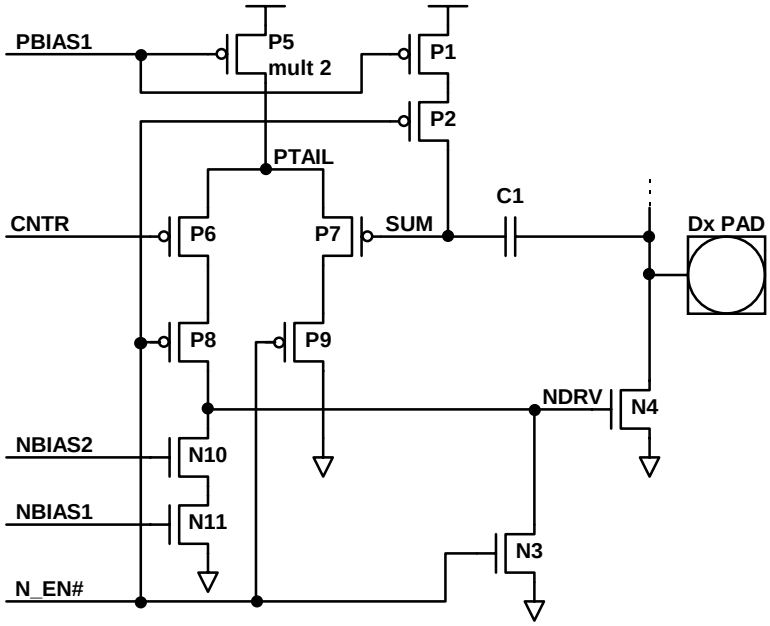


Figure 2-5 - Pull-down edge rate control circuit (extracted)

In this circuit, transistor P1 forms the current source for i_{SRC}. P1 is a current mirror controlled by BIAS cell output voltage PBIAS1 and delivers one unit of current. P2 is a current switch for i_{SRC} and is turned on when the buffer is transitioning low, enabled by N_EN#. The amplifier is a simple differential amplifier made up of transistors P5 through P9, and N10 and N11. Transistor P5 is the "tail" current source for the differential pair P6 and P7. (Since the "tail" of the amplifier is tied up to Vcc, this configuration is sometimes referred to as a "tail-up" differential amplifier.) P5 is made up of two identical transistors (hence the "mult 2" designation), each of which deliver a unit of current. The gate of P6 is the negative input and the gate of P7 is the positive input of the differential amplifier. P8 and P9 are current switches which enable and disable the amplifier (the EN# input in Figure 2-4). Finally, N10 and N11 make up the load transistors of the amplifier. N11 is a one unit current source controlled by BIAS cell output voltage NBIAS1. N10 is a cascode transistor for N11 and improves its performance as a current source and, therefore, the transition linearity. No load transistors are needed on the P7 side of the differential amplifier, since the output from that side is not used. N3 enables the output of the amplifier/predriver when N_EN# is low. As before, transistor N4 is the output buffer pull-down transistor. Capacitor C1 provides feedback from the pad to the input of the amplifier, node SUM.

A controlled, falling edge is produced as follows:

Initially, the PAD is in the high state with N_EN# also high. Since the pad is not moving, there is no current through C1. SUM is held near Vcc/2 by the clamping circuit. With N_EN# high, the current through the differential amplifier is cut off by P8 and P9 and N3 holds node NDRV low, keeping N4 off. The low-going transition starts when the N_EN# goes low, the differential amplifier is enabled, and N3 is turned off so that node NDRV can charge up. N_EN# enables P2 and allows P1's unit of current to charge node SUM. When SUM is above Vcc/2 (CNTR), differential pair transistor P7 shuts off and P6 is turned on such that most or all of the two units of current from tail current source P5 flows through P6 to node NDRV. N10 and N11 draw one unit away from NDRV, leaving a net of 1 unit of current to charge up NDRV.

When the voltage on NDRV crosses the threshold voltage of N4, N4 will begin to draw current, starting the negative transition on PAD. As soon as PAD starts to move, i_{CAP} will flow through C1 according to equation [1]. This current pulls against i_{SRC}, pulling SUM down. As SUM comes back towards Vcc/2, The current flow increases in transistor P7 and decreases in P6. As the P6 current decreases, the charging rate on NDRV slows. At the point that i_{CAP} balances i_{SRC}

and pulls SUM down to where the P6 current balances with the N11 current, the voltage on NDRV stabilizes and the transition rate on PAD is set. (In actual operation, the NDRV node will continue to rise slowly because N4 loses drive capability as its drain voltage drops.)

If the slope of PAD exceeds the target slope, i_{CAP} is greater than one unit, the net current into SUM is negative and the voltage on SUM drops. This unbalances the differential amplifier, reducing the current in P6 below one unit. This makes the net current flow into NDRV negative. The gate voltage on N4 decreases, acting to reduce the transition slope on PAD. A lower than target slope decreases i_{CAP}, raises the voltage on SUM, increases the net current into NDRV and drives the slope back up. This current balancing continues until the pad reaches ground. At this point, the slope is forced to be zero, no i_{CAP} flows, SUM is pulled up by i_{SRC} and all the current from P5 goes to NDRV. The gate on N4 starts charging again and eventually reaches about Vcc - 0.5 volts, giving full gate drive to N4.

The positive transition is controlled in the exact same manner using a second amplifier and associated current sources. Referring to Figure 2-2, i_{SRC} current is supplied by N1 and switched by N2. A “tail-down” differential amplifier is used. The configuration is the dual of Figure 2-5 and is shown in Figure 2-6. N5 is the tail current source and N6 and N7 are the differential input pair. N8 and N9 are the enables and P10 and P11 form the output load. The differential enables and transistor P3 are driven by P_EN. The output pull-up transistor is P4. Feedback current i_{CAP} from PAD to SUM is shared with the falling edge control circuits through capacitor C1.

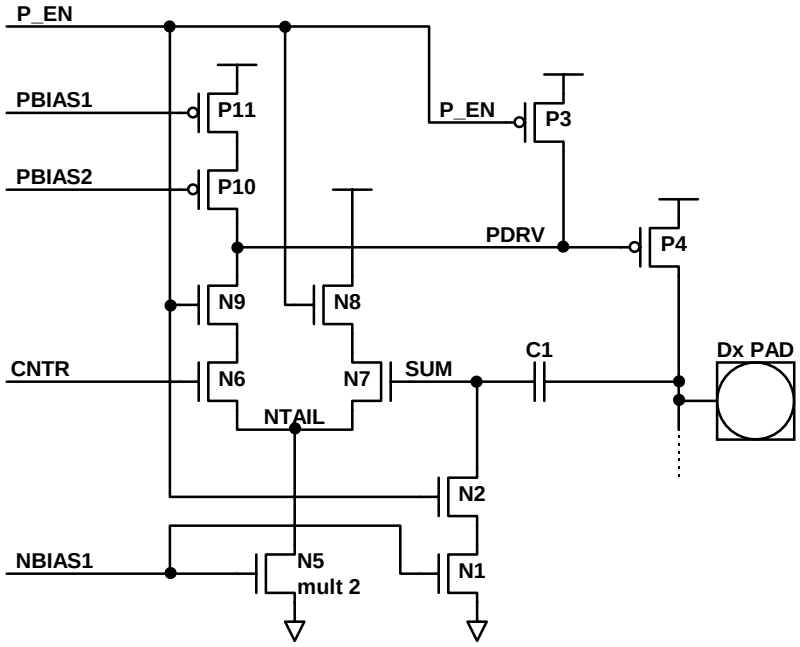


Figure 2-6 - Pull-up edge rate control circuit

2.2.4 SUM NODE CLAMP CIRCUIT

A clamp circuit is need on the SUM node to always keep it near to the virtual ground set at Vcc/2 by the BIAS cell signal CNTR. Without it, SUM would be pulled to the rail every time a transition completed and i_{CAP} dropped to zero. It would take too long for SUM to be pulled back to Vcc/2 so that the edge rate control circuit could function. The swing allowed by the clamp circuit is one component of the buffer gain and too wide a range can give a large gain which adversely affects buffer performance. The clamp circuit shown in Figure 2-7 limits the swing on SUM to a few tenths of a volt.

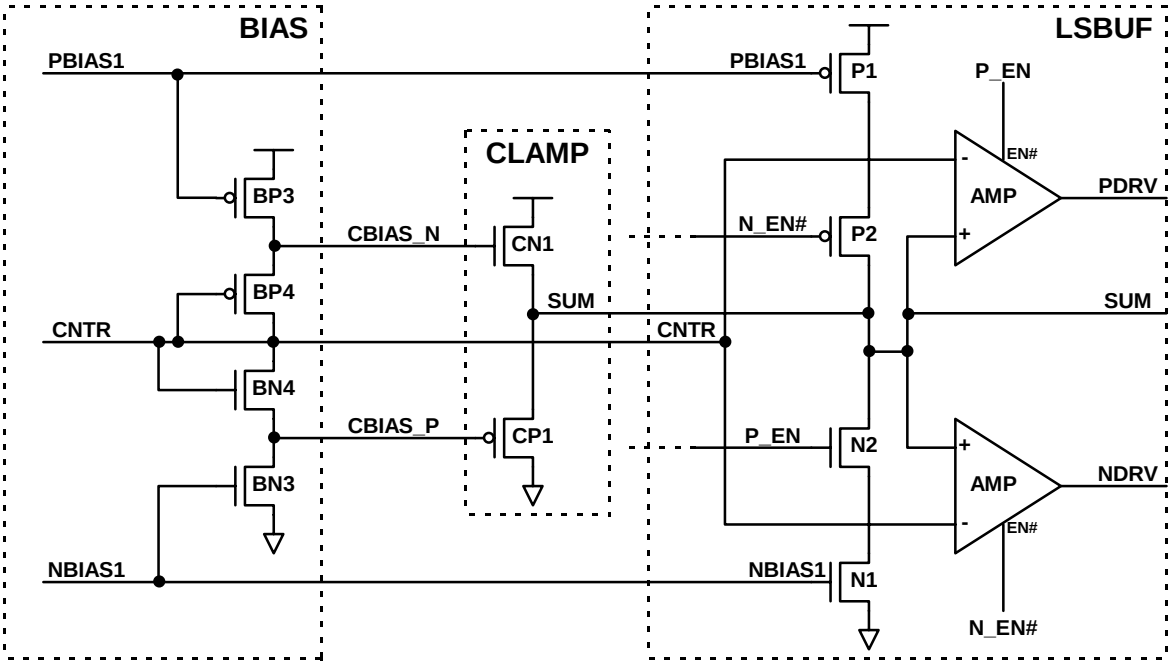


Figure 2-7 - CLAMP cell detail

CBIAS_P and CBIAS_N are set so that clamp transistors CN1 and CP1 are biased just below threshold when the voltages on SUM and CNTR are equal. At this point, CN1 and CP1 do not effect the currents flowing to or from SUM. If SUM moves too far negative of CNTR, CN1 will be turned on and will supply current to the SUM node to keep it from going lower. Similarly, if SUM goes too high, CP1 turns on and limits the positive swing on SUM. The clamp range is set just wide enough to give sufficient voltage input to the amplifiers for them to fully turn on or off the differential input transistors.

2.3 BIAS Cell Basic Operation

There are two sections to the BIAS cell: N/PBIAS and CBIAS .

2.3.1 CURRENT MIRROR REFERENCES

The N/PBIAS section creates the unit current needed to set the slope of the buffer output. It also creates the bias voltages that control the currents in the buffer predriver. The unit current is set by the value of the R1 - R4 resistor string and the voltage across it. Each end of the resistor string has a set of diode-wired (gate tied to drain) devices in series with it to act as reference devices for a current mirror. Transistor set BN1 forms bias voltage NBIAS1 that controls the currents through current mirrors BN3, N1, N5 and N11. All the transistors that make up BN1, BN3, N1, N5 and N11 are identical in size. Similarly, transistor set BP1 forms voltage PBIAS1 and sets the current in current mirrors BP3, P1, P5 and P11; with all of these transistors identical to each other. Whatever current is conducted in each transistor of the reference set will be reflected in each transistor in the mirrors.

The current desired in the sources is only in the range of 20 μA, so it would take a physically large resistor to set such a small current. The resistor value (and area) can be reduced by using a set of identical devices in BN1 and BP1. The current will be set so each individual device carries only one unit of current. In the example cell of Figure 2-3, five transistors are used per reference set and the current through them is set to about 5 units of current (≈100 μA). Device BP2 shuts off the current through the N/PBIAS section and BN2 ties the network to ground when the BIAS cell is disabled (BIAS_EN# is high).

The resistors R1 through R4 divide the voltage across them such that node CNTR is at half Vcc and that the voltage across R1 and R4 are about 0.5 volts. R1 and R4 set bias voltages NBIAS2 and PBIAS2 respectively. These voltages control the cascode voltages for the current mirrors discussed above.

2.3.2 REFERENCE FOR SUM NODE CLAMP CIRCUIT

The CBIAS section sets the CBIAS_N and CBIAS_P voltages such that CN1 and CP1 are cutoff by one or two tenths of a volt when the node SUM is held around Vcc/2. Current mirror BN3 draws current through diode-wired device BN4, setting CBIAS_P at about an N-device threshold below CNTR (Vcc/2). Similarly, BP3 biases device BP4 to set CBIAS_N at about a P-device threshold above CNTR. The transistors in the CLAMP cell have more source voltage than the devices in BIAS (have more body effect), therefore have slightly higher thresholds. This tends to make CN1 and CP1 nearer their cutoff region than BN4 and BP4, which is the desired bias state for CN1 and CP1. The sizes of BN4 and BP4 and the current through them can be adjusted to fine tune the conduction of CN1 and CP1. The currents through BN4 and BP4 must be well matched such that no current flows from them to node CNTR and upsets the resistor currents.

2.4 Enhancing Buffer Performance

2.4.1 REDUCTION OF BUFFER DELAY

The low current in the predriver cell causes the output buffer not to begin to switch until the current can charge the output driver's gate node (NDRV or PDRV) sufficiently to begin conduction. This "dead time" can be reduced by pumping the gate up faster to about the driver's gate threshold. Figure 2-8 shows a method for reducing dead time. Transistors N12 and P12 are wired as source followers using NBIAS2 and PBIAS2 as reference voltages. P13 and N13 switch on N12 and P12 when that side of the buffer is enabled. When enabled, N12 or P12 quickly pulls NDRV or PDRV up to about 0.5 volts. At that point, the transistor cuts off and the normal currents into the driver's gate node take over to control the gate voltage. The initial gate charging time is almost eliminated and the dead time is reduced significantly.

There is a limit as to how much the follower can pull up the gate before there are detrimental effects. If the gate is pulled too high, the driver will turn on more than it is intended to and will start the transition too soon and with too fast a slope. The buffer slope controls will be defeated in this case. The gate can be pulled only as high the lowest gate drive necessary to start a transition. Some margin to this case should be allowed for safety. Note that the bias voltage to N12 and P12 is set by the resistors and does not track transistor parametrics.

2.4.2 COMPENSATING FOR THE USB PULL-UP RESISTOR

The above circuit works very well into a capacitive load over a range of 50 to 350 pF as required by the USB specification. However, the load on a low speed buffer is not entirely capacitive. There are 15 KΩ pull-downs on both data lines and a 1.5 KΩ pull-up resistor the D- data line. The pull-down resistors are not a problem. However, with light capacitive loads, the pull-up resistor creates an initial slope which is much faster than the target slope. This creates an i_{CAP} which is larger than target and acts to shut off the output driver in an attempt to slow the edge rate. The driver will remain off until the edge rate of the exponential R-C at the output falls below the target edge rate, at which point, the edge control circuitry kicks in and regulates the remainder of the rise time. The faster initial slope causes the rising and falling edges to be badly mismatched for the K-state to J-state transition, which introduces unacceptable data skews.

The solutions to this problem lies in providing a load to the pull-up transistor in the low speed buffer such that it is conducting current throughout the rise time of the data line. This can be accomplished either by providing sufficient capacitive load such that the rise time, even with the pull-up resistor is slower than target, or by providing a pull-down current in the buffer that balances the current from the pull-up resistor. The first method works for low speed devices on their root ports where capacitive loads can be guaranteed. The second method is suited for downstream hub ports.

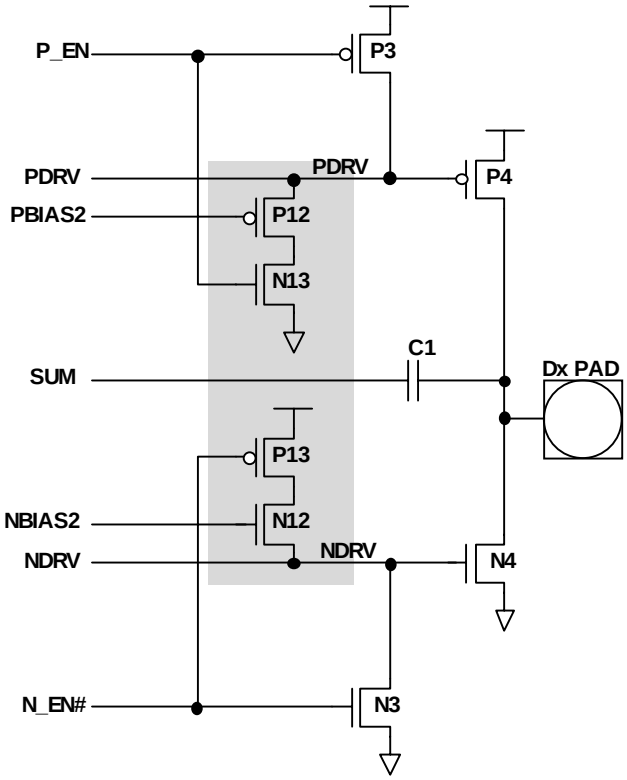


Figure 2-8 - Method to reduce buffer delay by reducing dead time

2.4.2.1 Minimum capacitive loading

The minimum capacitive load method works by reducing the initial edge rate on the D- data line caused by the pull-up resistor. At the start of the rising edge, the pull-up provides about 2.5 mA into the load capacitance. The minimum load capacitance can be found by using equation [1] and the target edge rate.

$$C_L(\min) = \frac{V_{CC}(\max)}{R_{PU} * Slope} \qquad [2]$$

Assuming a maximum Vcc of 3.6 volts and a target slope of 20 V/µs, the minimum capacitive load is:

$$C_L(\min) = \frac{3.6V}{1.5K\Omega * 20V / \mu s} = 120pF$$

At 120 pF loads or greater, the slope caused by the pull-up resistor are always less than the target slope and the pull-up transistor in the low speed driver will have to turn on and provide current to meet the target slope. This capacitive load can be met by a typical cable of 3 to 4 feet. However, low speed cable capacitances can vary significantly and the range of possible loads should be verified.

2.4.2.2 Current loading

The initial slope of the D- line can also be modified if the net current into the capacitive load is reduced. This can be done by having the low speed buffer pull current from the load during the rising edge. The amount of this current can also be calculated by using equation [1]:

$$i_{LOAD} = \frac{V_{CC}(\max)}{R_{PU}} - C_L(\min) * Slope \qquad [3]$$

For the specified minimum load of 50 pF and a target slope of 20 V/µs:

$$i_{LOAD} = \frac{3.6V}{1..5K\Omega} - 50pF * 20V/\mu s = 2.4mA - 1.0mA = 1.4mA$$

A value of 1.4 mA insures that P4 is pulling up against the current load for the entire swing, but in practice any value between 1.0 and 2 mA is sufficient. The current load can be generated in the buffer by turning the output pull-down transistor N4 on D- into a current source during the rising edge. Instead of turning off N4 during the rising edge, the gate voltage is held at a level that causes N4 to sink i_{LOAD}. Since it is not desirable to draw this current constantly, N4 must eventually be switched off.

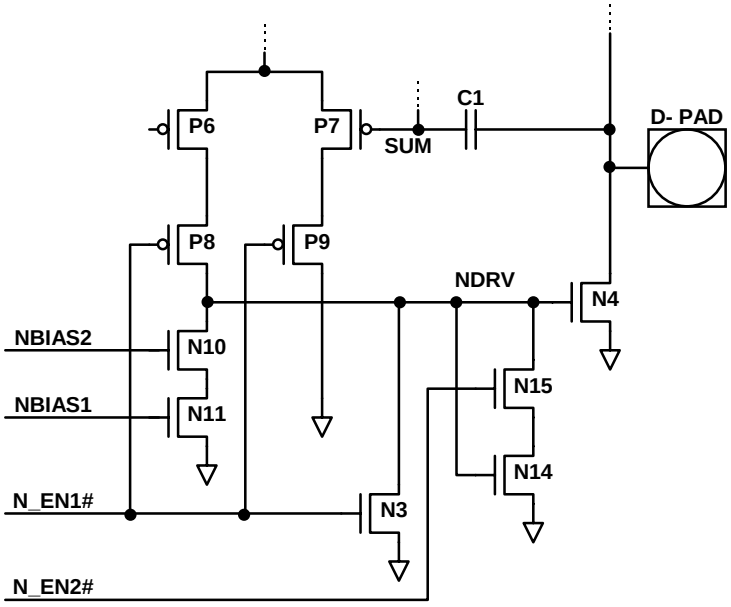


Figure 2-9 - Adapting the low speed buffer to produce a load current

Figure 2-9 shows an example design for adapting the pull-down driver to provide a load current. Two transistors, N14 and N15, and a second enable signal N_EN2# have been added. Transistor N14 is diode-wired as a current reference, with N15 in series. N_EN2# switches N15 off. Figure 2-10 shows how the two buffer enables are controlled. N_EN2# is switched as in a normal buffer control. N_EN1# is low when the buffer is to be low, but its rising edge is delayed until the data lines have crossed. The crossing point can be detected by the buffer's own differential input receiver.

During the time that N_EN1# is low and N_EN2# is high, current from transistor P5 is still flowing via P6 and P8 into node NDRV, but the voltage level is clamped by N14. N14 now acts like a current mirror reference diode (like BN1 in BIAS), with output transistor N4 as its mirror device. The current mirrored in N4 during this time depends on the geometric ratio of the sizes of N4 over N14. If N14's channel length is the same as N4's, then the current mirrored in N4 is the ratio of the change widths of N4 over N14. In order to get the 1.0 to 2.0 mA needed as a load current, the ratio of N4/N14 must be I_{LOAD}/I_{UNIT}. For the currents in the example design, this requires a size ratio of 50 to 100. (There are practical limits to the size of N14. See Design Cookbook.)

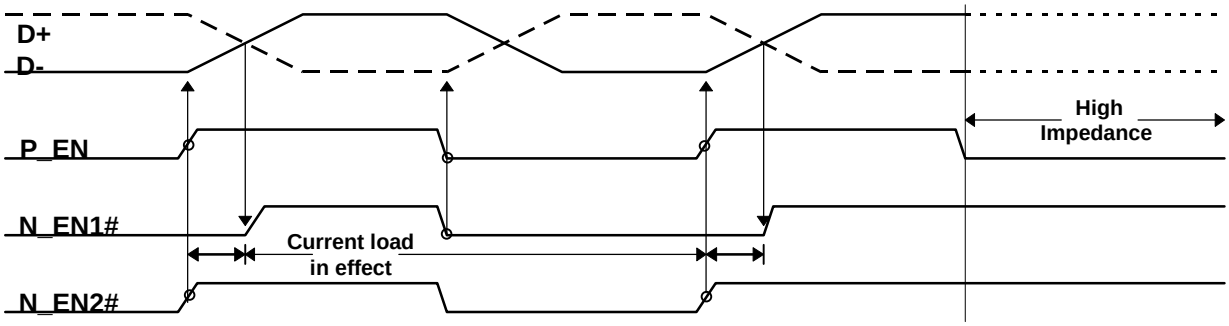


Figure 2-10 - Waveforms for N_EN1# and N_EN2# control signals

Note that using the differential input buffer as a means to control the timing of N_EN1# has some key advantages. First, it provides a way to shut off the current load at the earliest convenience of the circuit, saving power. Second, it controls the rise time until the data lines cross, insuring that the differential data skew is minimized.

3. BUFFER DESIGN COOKBOOK

The design of the low speed buffer proceeds with the following steps, which are described in detail in the next sections:

1. Select process specific devices and sizes (Z's and L's, etc.).
2. Select C1 feedback capacitor value and calculate the unit current.
3. Set the size of the output transistors (N4 and P4) based on AC and DC load currents.
4. Set proper gate drive for diode-wired reference devices in N/PBIAS circuit.
5. Setup N/PBIAS circuit section and set total value of current with sum of R1-R4.
6. Select R1, R2, R3 and R4 ratios to get proper NBIAS2, CNTR and PBIAS2 voltages.
7. Set CBIAS_ N and CBIAS_P to set transistors CN1 and CP1 at edge of cutoff/conduction.
8. Size the differential amplifier.
9. Add performance enhancements.
10. Final simulation, tweaks of currents and sizes, and verification over process, temperature and voltage.

3.1 Select Devices And Sizes

The theory of operation section assumes ideal devices and operation. There are several real process issues that have to be considered before design starts. The choices made here will affect the performance of the final design. This design depends on the existence of a reasonably stable and voltage independent capacitor and resistor to set the slope of the output rise and fall time. It also depends on reasonable matching between the reference devices in the BIAS cell and the current mirrors they drive.

3.1.1 DEVICE PARAMETERS VERSUS BUFFER PERFORMANCE

The performance of the buffer is measured by its ability to stay within the specified rise and fall times of 75 ns to 300 ns and by the matching of the slopes and the voltage point where the two data lines cross. To the first order, the rising and falling edge rate is set by the current in the feedback capacitor C1 and in the current mirrors N1 and P1. The mirror currents are set by the resistors R1-R4 and the Vcc supply voltage. Therefore, predictable rise and fall times depend largely on having an R and C circuit elements that are stable over process, temperature and voltage.

Matching the rising and falling slopes mostly depends on matching the currents in the predriver. The capacitor current is common to both rising and falling edges, so the matching largely depends on the matching of the current mirrors themselves. Transistor matching is done through device size choices and layout techniques that are not dependent process, temperature and voltage (at least as long as the bias voltages are within reasonable limits).

There are some second order effects which affect the matching of the timing of the two edges. The capacitance of the internal nodes causes some loss of efficiency. The output driver gated nodes PDRV and NDRV require attention to be sure that their capacitive loading and coupling from the PAD are closely matched. Also, the biasing on CP1 and CN1 must be set so that when an edge is in progress, there is sufficient voltage swing to drive the differential amplifier, the swing is not too great that the recovery time at the next edge is too large and when the voltage on SUM is close to CNTR, there is little loss of current into the clamp transistors that could distort the edge rate control.

3.1.2 R'S AND C'S

The value of R1-R4 are in the several kilohm range. Using the well layer is usually a good choice since the resistance is in the few hundred ohm to few kilohm range per square. It is often a fairly stable resistance since it sets the device characteristics of the transistor built in it (although the temperature coefficient is higher). This paper assumes N-well technology, but any isolated well works. N-well resistors are best built as strips of wells with N+ well taps at the end. Matching is done by laying strips of identical width side by side and setting value by ratio of length. Matching is enhanced by making the strips of greater than minimum width and spacing (1.5X spacing and more than 2.0X width).

The value of C1 is usually set to around 1 pF. Transistors have the largest capacitance per unit area of any device, but are generally unsuitable for this application because of the high voltage dependence on the capacitance and large parasitic capacitances. The most stable capacitor is a poly-metal-metal sandwich. This type of capacitor takes significant area, but it is stable over process and when the middle of the sandwich is used for the SUM feedback node, there is good shielding for the node and minimal parasitics. The capacitor should be laid out as square as is practical to

minimize process variations and noise pick-up. Overlapping the center plate with the outer plates and keeping other signals away from the center plate reduces crosstalk to the SUM node.

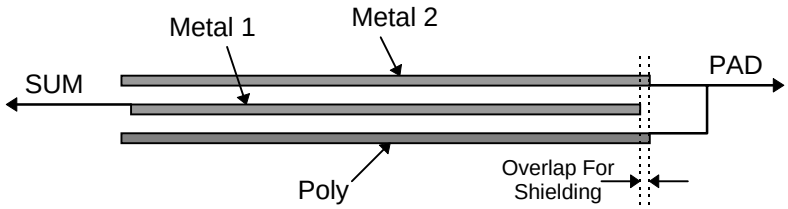


Figure 3-1 - Poly-Metal-Metal sandwich for feedback capacitor

3.1.3 TRANSISTOR MATCHING

The only transistors for which matching is critical are the BIAS reference transistors and the current mirrors. The other devices (except the output buffer transistors) can be sized using the minimum L and a moderate strength W (10 μm to 20 μm). The W for N and P transistors should be ratioed such that they have about the same drive strength for equivalent operating conditions. Output buffer transistor sizing should follow process design rules for channel length and increments of channel width.

Transistor matching is determined by sizing and layout. Both the W and L dimensions must be much greater than minimum in order to swamp out any processing irregularities. Factors of at least three to five times minimum are recommended. Matched devices are laid out in identical fashion. If the device has to be two times or five times bigger than a other devices, it is made from two or five identical devices, not from a device with a W that is longer. Also, matched devices must be laid out in the same orientation as each other. This means that they are all laid parallel and with the source and drains in the same orientation. Finally, the matched devices must share the identical power supply rails so that there is no offset voltage between the sources of the reference and current mirror devices.

3.2 Select Feedback Capacitor And Calculate The Unit Current.

Selection of the capacitor sets the unit currents. Larger currents make the design more noise resistant and require a smaller area of resistors, but require larger capacitors. Also, higher currents make the bandwidth of the amplifier higher and tends to make the circuit less damped. The trial designs found that a value 1 pF for the feedback capacitor gives satisfactory results. As calculated in section 2.2.2, a capacitor of 1 pF gives a unit current of 20 μA.

3.3 Set The Size Of The Output Transistors

The size of pull-down output transistor N4 can be determined by simulation using a static load current to meet the output low voltage specification (V_{OL}) of 0.3 volts under worst case conditions. N4 must be able to sink enough current to discharge the maximum capacitive load plus the DC load of the USB 1.5 KΩ pull-up transistor. The DC load is 2.4 mA (3.6 V/1.5 KΩ). The AC load is calculated by equation [1] where C is 350 pF and the slope is 20 V/μs. This yields an AC load of 7.0 mA or a total load of 9.4 mA (~10 mA). In order for the predriver circuit to be operational, the gate voltage on N4 must be about 0.7 volts below the minimum Vcc. Simulations should be run to find the size of transistor that can sink a 10 mA load with a gate drive of Vcc(min)-0.7 volts that can just meet the V_{OL} of 0.3 volts under worst case (low supply voltage, slow process, hot temperature) conditions:

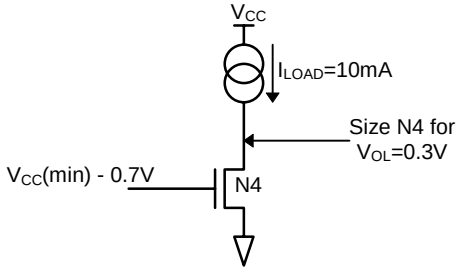


Figure 3-2 - Pull-down output transistor sizing simulation circuit.

The size of N4 should be rounded up to the next convenient increment for the output driver layout sizes dictated by the library and design rules being used. The size of P4 can be derived by ratio form the size of N4, such that P4 has equivalent drive strength as N4 under the same conditions. N4A (see Figure 2-2) is sized to be the difference in size between N4 and P4 such that the node capacitance on the NDRV and PDRV is the same.

3.4 Set Gate Drive For Reference Devices In N/PBIAS

Figure 2-1 shows a method for determining the size of the reference devices in the BIAS cell. The drain current is swept from zero to two units of current. The resulting V_{GS} curve shows the transistor threshold V_T and the gate drive (V_{GS} - V_T) on the transistor for various currents through the transistor. The proper size of reference device transistor should have about 0.3 volts of gate drive with one unit current flowing through it. This insures that the device is in strong inversion, has sufficient drive on its gate to resist threshold shifts, but is low enough to operate with the bias points set in this buffer design.

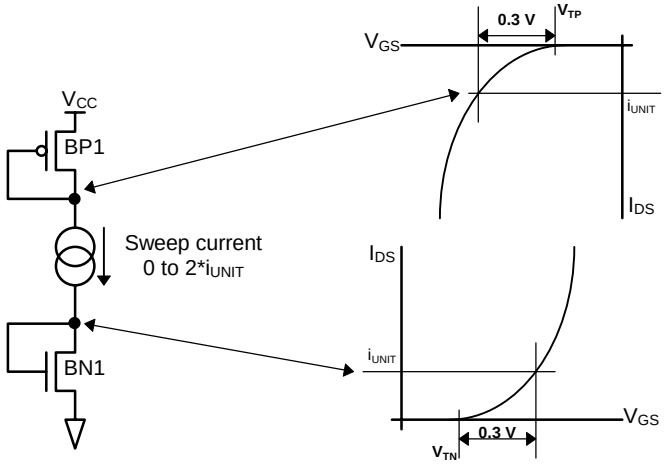


Figure 3-3 - Setting gate drive for reference devices in BIAS cell

This is a point where practical issues should be considered. First, be sure that the chosen device sizes for the transistor in BN1 and BP1 meet the matching standards discussed in section 3.1.3. Also, there are current losses in the predriver due to charging parasitic capacitances and charge sharing through the output drive to the pad. These losses are 5% to 10%. An extra 10% can be added to the unit current during these simulations and in the next section to compensate.

3.5 Set Value Of Devices in N/PBIAS Section Current

The key decision in setting the device sizes in the N/PBIAS circuit is the amount of DC current that is used in BIAS. Larger currents mean higher quiescent power and more reference device transistors in BIAS, but also allow smaller area resistors (R1-R4) and faster recovery from the low power state (when OE# and B_EN# are high in Figure 2-1). More transistors will improve matching between the BIAS reference device and the LSBUF current mirrors as process irregularities will be averaged out in the BIAS transistors.

At least one unit of current has to flow in the N/PBIAS section of BIAS. The current can be increased in increments of the unit current. For each increment, the value of the resistor is reduced and another transistor is added to the set in BN1 and BP1. This example design uses five units of current in N/PBIAS as a reasonable balance of quiescent current and recovery time.

The total value of the resistors in N/PBIAS is set by:

$$R_{TOTAL} = \sum (R_1 - R_4) = \frac{Vcc(nom.) - (V_{GS}BN1 + V_{GS}BP1)}{N * i_{UNIT}} \qquad [4]$$

Where Vcc(nom.) is the nominal supply voltage (assumed to be 3.3 volts), V_{GS}BN1 and V_{GS}BP1 are the gate to source voltages obtained from the simulations in the last section and N is the number of units of current chosen (5 in this example design). Again, the 10% current loss factor should be applied here for initial sizing and can be adjusted later. Assuming V_{DS} for BN1 is 0.9 V and V_{DS} for BP1 is 1.0 V, the result of equation [2] for this design is a total resistance of 12.7 KΩ.

3.6 Set Proper NBIAS2, CNTR And PBIAS2 Voltages

The sizes for R1 through R4 can now be calculated to set the values of the remaining bias voltage from the N/PBIAS section of BIAS. CNTR can be put close to Vcc/2 by making (R1 + R2) = (R3 + R4). This also implies that (R1 + R2) = 0.5R_{TOTAL}. The voltage drop across R1 and R4 should both be about 0.5 volts, so R1 = R4 and also R2 = R3. R1 can be obtained directly by dividing the targeted voltage across R1, V(R1), by the current through it, N*i_{UNIT}. This yields the equations for setting the resistors sizes as:

$$R_1 = \frac{V(R_1)}{N * i_{UNIT}} \qquad [5]$$

$$R_2 = 0.5 * R_{TOTAL} - R_1 \qquad [6]$$

$$R_3 = R_2 \qquad [7]$$

$$R_4 = R_1 \qquad [8]$$

For the example case, R1 and R4 are about 4.5 KΩ, and R2 and R3 are about 1.9 KΩ.

3.7 Set CBIAS_ N And CBIAS_P Voltages

The circuit of Figure 3-4 can be used to help set the bias voltages CBIAS_N and CBIAS_P. The N/PBIAS circuit developed in the preceding sections supplies the bias voltages PBIAS1, CNTR and NBIAS1. The initial transistor sizes are set as follows. BN3 and BP3 are sized the same as one transistor in the set of their respective reference devices BN1 and BP1, respectively. BN4 and CN1 are the same size, as are BP4 and CP1.

The initial simulation is run until the node voltages and currents stabilize. Then the SUM node is swept very slowly from Vcc/2 - 0.3 V to Vcc/2 + 0.3 V and the currents in CN1 and CP1 are examined. The desired outcome is that the currents through CN1 and CP1 do not overlap, and that at the voltage gap between the conduction points is about ±300 mV at one unit of current, as shown in Figure 3-5. The current may have to be adjusted in final simulations to properly set the buffer gain. The gap should be centered roughly around CNTR.

If the gap in conduction is not correct, then the voltage between CBIAS_N and CBIAS_P has to be adjusted to compensate. This can be done by increasing or decreasing the current through BN4 and BP4 by adjusting the number of transistors in BN3 and BP3 or changing their W appropriately. BN4 and BP4 can be resized to change the voltage drop across them. A warning: any change that makes the L's and Z's mismatched between component devices will

cause the relative performance to vary more over process. Verify these changes carefully. Also, whatever changes are made, the currents through the CBIAS section have to be balanced such that little or no current flows through CNTR back into the N/PBIAS section.

If the slope of the current as it leaves the crossover point is not correct, then the size of the clamp transistors can be adjusted. Again W or L, or the number of parallel transistors can be changed. Use the same care in selection and verification as described above.

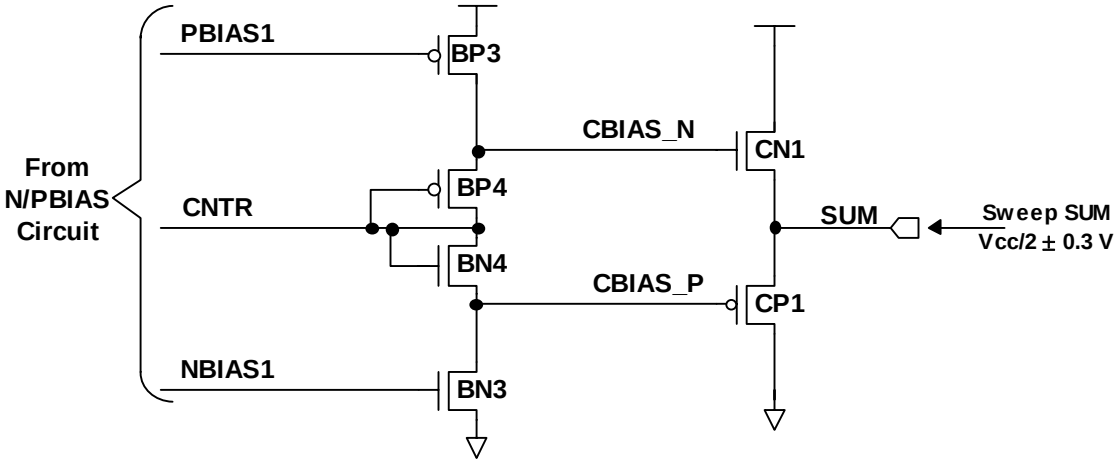


Figure 3-4 - Simulation model for setting CBIAS_N and CBIAS_P

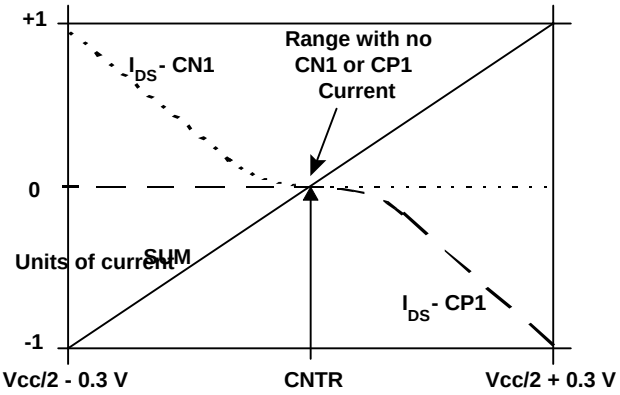


Figure 3-5 - Desired initial results for CN1-CP1 current simulations

3.8 Set Up Differential Amplifier

This is the most difficult part of the circuit. Too much gain will cause ringing in the gate drive of the output transistors (NDRV and PDRV) and distortions in the output waveform. Too little gain results in poor slope control as well. Gain is controlled by the current in the differential amplifier tail transistor (P5 and N5), the sizes of the differential input transistors (P6, P7 and N6,N7) and by the clamp circuit response. Any of theses can be tweaked to change the system gain. Ringing on the NDRV or PDRV nodes is a sign system gain is too high. There is one exception to this. If the design includes the compensation circuit for the pull-up resistor, the PDRV signal in the D- buffer will change value when the compensation circuit is switched out. (See simulations in the Appendix.)

The two differential amplifiers should have sufficient gain such that the range of the clamp circuit can be small and still allow the differential output to swing from no current delivered to NDRV to all the tail current delivered to NDRV. The suggested target is no more than a 300 mV swing in either direction should be required to fully turn on or off the current through either differential input transistor.

The current in the load transistors (N11 and P11) need to be set to one half of the tail current. This is most easily done by using two transistors in parallel for P5 and N5 compared to one transistor for N11 and P11. The current in the tail (P5 and N5) sets the bandwidth of the amplifier. Insufficient current will make the edge rate control too sluggish. Too much current will make it less stable.

3.9 Add Performance Enhancements

The delay reduction (N12-13 and P12-13) and pull-up compensation circuits can be added at this point. The voltage at NBIAS2 and PBIAS2 may have to be adjusted to give the best results. The voltages should be set individually to bring the NDRV and PDRV up to a point at which the output driver is not quite turned on. This has to be checked at the worst case corners to be sure that the buffer is not turned on and the slope control is not overridden by these circuits.

The pull-up compensation circuit needs to be tuned to get 1.0 mA to 1.4 mA in N4 during the rising edge transition on D-. This requires a strength ratio of 50 to 100 between N4 and N14. It is recommended that N14 have the same channel length as N4 for best matching over all conditions. Also, N14 should be laid out close to N4 and it should share the same ground as N4.

For the design example given at the end of the paper, the output buffer is 300 μm. To get a minimum ratio of 50:1, N14 would have to be 6 μm. This is a bit small for good matching. Larger transistors can be stacked in series, with the gates tied to the same node, to get a larger ratio while preserving reasonable matching. The design example stacks two 10/1.0 μm transistors to get the desired performance,

3.10 Final Simulations and Verification Over Process, Temperature And Voltage

All the sizes for the buffer are now determined. Simulations can be run with these sizes. The load capacitance should be run from 50 pF (min. load) to 350 pF (max. load). Also include the 1.5 KΩ pull-up and 15 KΩ pull-down resistors that are on USB. The results should be checked for good matching of rise and fall slopes and delays and matching of bias currents and voltages. The actual slope can be tweaked to meet 150 ns rise/fall time by scaling the values of R1-R4.

If the rise time does not match the fall time, recheck the current matching. Check that during transitions, that the voltages and currents in the clamp circuit are symmetrical around CNTR and the currents through N8 and N10 are close to the currents in P8 and P10. Also, there is a possibility that the gate to drain capacitance in N4 does not match P4 and there is different capacitive coupling charge loss. Adding some gate to drain capacitance in place of N4A can compensate for a significant mismatch.

Also, the dv/dt of the pad should be watched to be sure that there are no significant transients or excessive ringing in the slope that may indicate marginal stability. If the gain of the amplifier is too high the unit current has to be scaled back.

All simulations should be run over process, voltage and temperature variations. Make sure the temperature coefficient of the well resistors is included. The same conditions as above should be checked.

4. BIBLIOGRAPHY

The following texts contain information on analog design (differential amplifiers, current mirrors, cascodes, etc.) that is useful in understanding this buffer.

P. Allen, D. Holberg, “CMOS Analog Circuit Design,” Holt Rinehart & Winston, 1987

P.R. Gray, R.C. Meyer, “Analysis and Design of Analog Integrated Circuits,” 3rd ed., John Wiley & Sons, 1993

R. Gregorian, G. Temes, “Analog MOS Integrated Circuits for Signal Processing,” John Wiley & Sons, 1986

5. REVISION HISTORY

Revision 0.0 - February, 1996 - Pre-release version.

Revision 1.0 - May, 1996 - Added Design Example in Appendix A

Revision 1.1 - December, 1996 - Modified to differential amplifier design

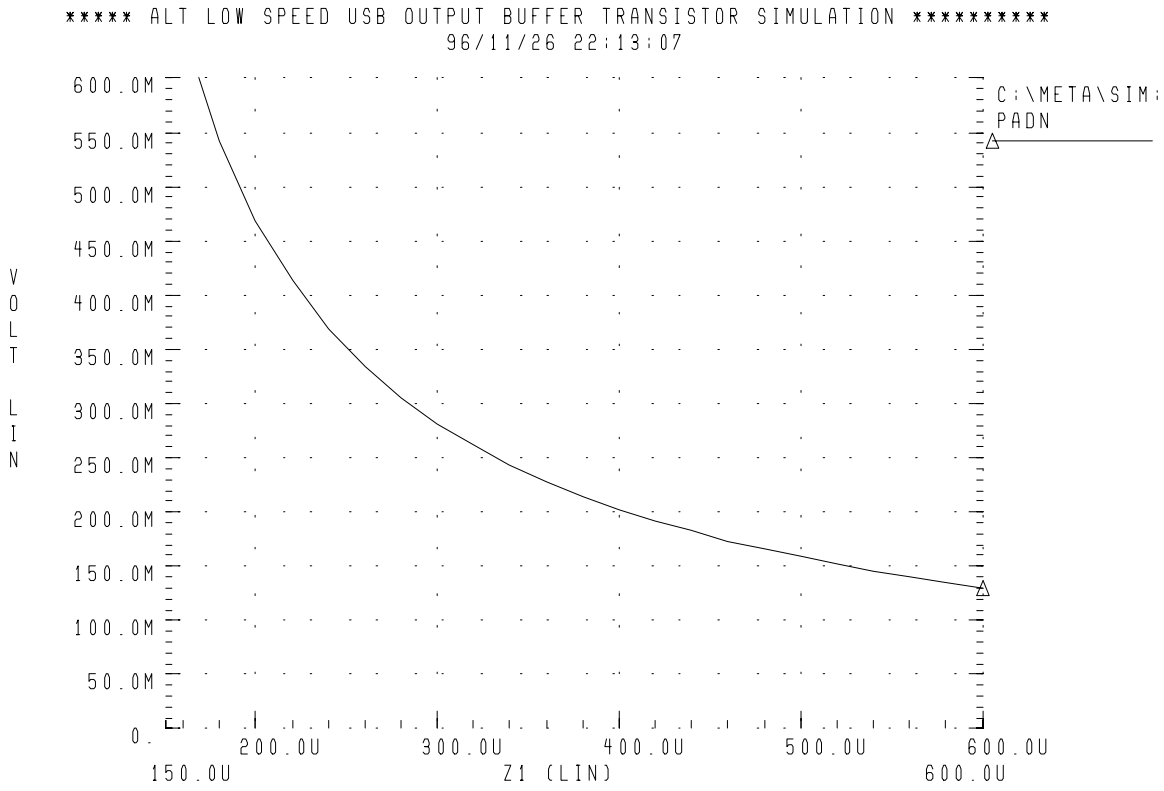
APPENDIX A. DESIGN EXAMPLE

The following sections show a series of HPSICE[1] simulations and HSPLOT outputs that follow the cookbook steps to design a USB low speed buffer. The design was done in a proprietary 0.8µm process.

Simulation to Set Output Buffer Transistor Sizes

```
***** Alt Low Speed USB output buffer transistor simulation **********
**********************************************************************
.LIB 'std08u.lib' EE
**********************************************************************
.DC Z1 100u 1000u 20u
.TEMP 100
.PRINT   DC  V(PADN) V(PADP)
**********************************************************************
VCC3  VCC  0    DC=3.0V
VGND  VSS  0    DC=0.0V
VGSN  NDRV 0    DC=2.3V
VGSP  PDRV 0    DC=0.7V
IOL   VCC  PADN DC=10.0mA
IOH   PADP VSS  DC=10.0mA
.DCVOLT PADN=1.0V PADP=1.3
**********************************************************************
MN8   PADN NDRV VSS VSS NCH W=Z1 L=1.0u
MP8   PADP PDRV VCC VCC PCH W=Z1 L=1.0u
**********************************************************************
.END
```

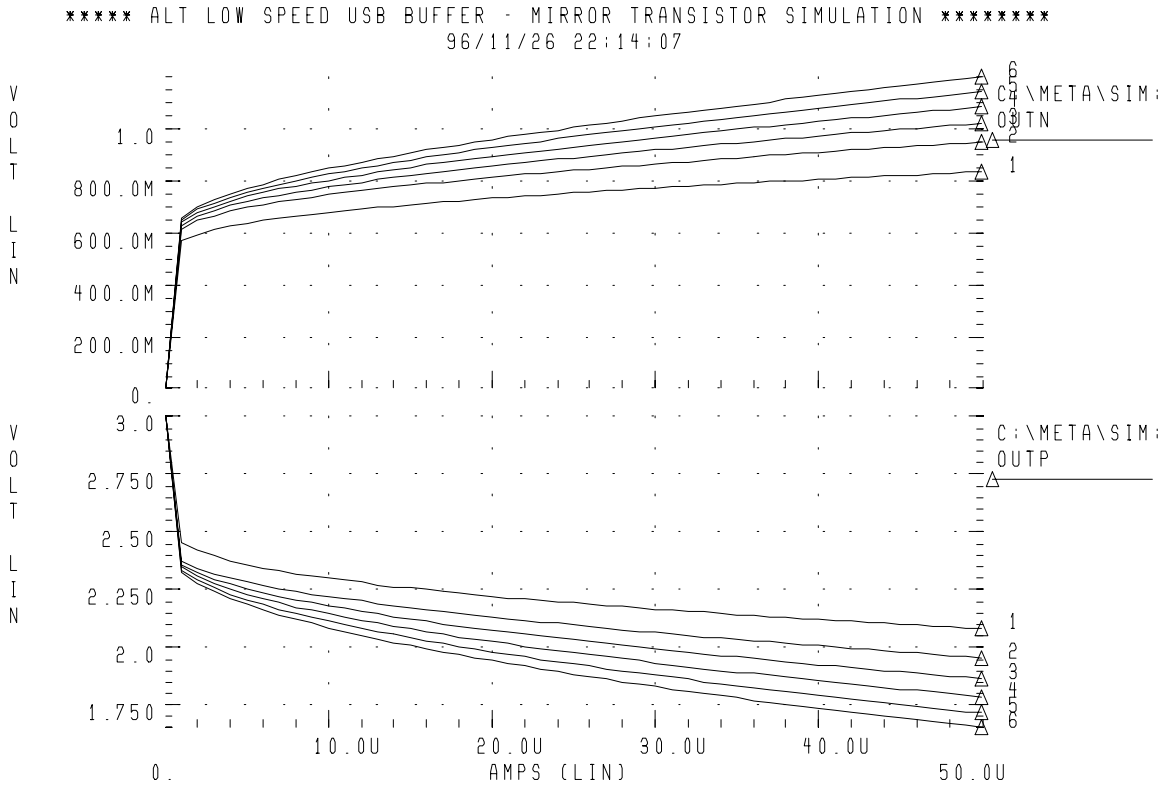
[1] HSPICE and HSPLOT are trademarks of Meta-Software, Inc.



The size for the N-channel output buffer transistor (N4) was found by simulating a range of transistor sizes with a current load of 10 mA. In this case, the VOL of 0.3 volts was reached at a transistor size of 280 µm. This was rounded up to 300 µm to give some margin to spec. The P-channel output transistor (P4) size was found by known ratio for transistor strengths of 2.5:1, or 750 µm.

Simulation to Set Mirror Transistor Sizes

```
***** Alt Low Speed USB buffer - Mirror transistor simulation ********
**********************************************************************
.LIB 'std08u.lib' EE
**********************************************************************
.DC IUNIT 0 50UA 1UA L2 1.0U 3.5U 0.5U
.TEMP 25
.PRINT   DC  VGSN=V(OUTN)
+            VGSP=V(OUTP)
**********************************************************************
VCC3  VCC  0    DC=3.0V
IUNIT OUTP OUTN DC=20UA
VGND  VSS  0    DC=0.0V
.DCVOLT  OUTN=0V OUTP=3V
**********************************************************************
MN1   OUTN OUTN VSS VSS NCH W=10U L=L2
MP1   OUTP OUTP VCC VCC PCH W=25U L=L2
**********************************************************************
.END
```



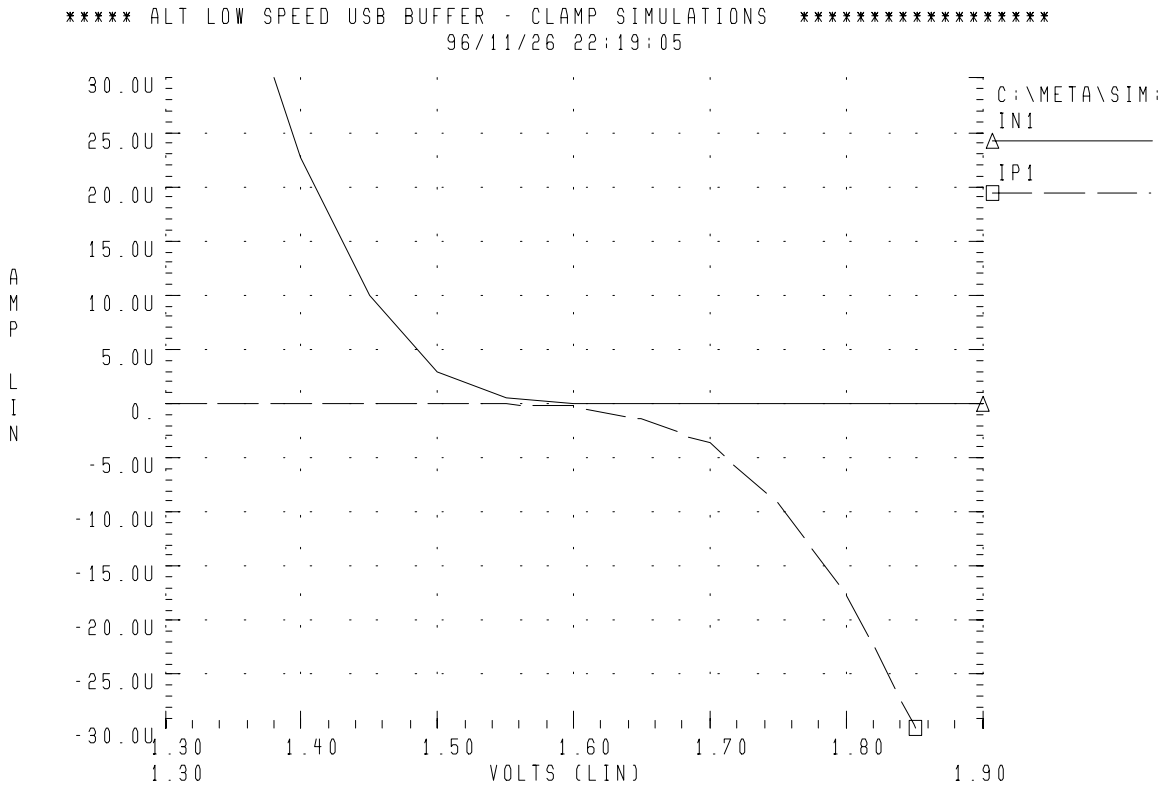
Transistor sizes (in (m) versus curve:

OUTN:	1 - 10/1.0	2 - 10/1.5	3 - 10/2.0	4 - 10/2.5	5 - 10/3.0	6 - 10/3.5
OUTP:	1 - 25/1.0	2 - 25/1.5	3 - 25/2.0	4 - 25/2.5	5 - 25/3.0	6 - 25/3.5

This simulation was used to find a transistor size (channel length) that gave about 0.3 volts of gate drive at 22 µA (20 µA + 10%) of drain current. Channel lengths of 2.5 µm satisfy this requirement.

Simulation of BIAS Cell and to Set CN1 and CP1 Transistor Sizes

```
***** Alt Low Speed USB buffer - Clamp Simulations  ******************
**********************************************************************
.LIB 'std08u.lib' EE
**********************************************************************
.DC VSUM 1.3V 1.9V 0.05V
.TEMP 25
.OPTION DEFL=0.8U
.PRINT DC    VNBIAS1=V(NBIAS1)
+            VNBIAS2=V(NBIAS2)
+            VPBIAS1=V(PBIAS1)
+            VPBIAS2=V(PBIAS2)
+            VCBIASN=V(CBIASN)
+            VCBIASP=V(CBIASP)
+            VCNTR  =V(CNTR)
+            VBND1  =V(BND1)
+            VNBIAS2=V(NBIAS2)
+            IR2    =I(R2)
+            IR3    =I(R3)
+            IBN3   =I(MBN3)
+            IBP3   =I(MBP3)
+            IN1    =I(MN1)
+            IP1    =I(MP1)
**********************************************************************
VCC3  VCC  0    DC=3.3V
VGND  VSS  0    DC=0.0V
VBENB BENB 0    DC=0.0V
VSUM  SUM  0    DC=1.6V
**********************************************************************
**  BIAS cell
**********************************************************************
MBN1  NBIAS1 NBIAS1 VSS    VSS NCH W=10U L=2.5U M=5
MBN2  NBIAS1 BENB   VSS    VSS NCH W=10U
MBN3  CBIASP NBIAS1 VSS    VSS NCH W=10U L=2.5U
MBN4  CNTR   CNTR   CBIASP VSS NCH W=10U        M=2
*
MBP1  BND1   PBIAS1 VCC    VCC PCH W=25U L=2.5U M=5
MBP2  PBIAS1 BENB   BND1   VCC PCH W=25U        M=2
MBP3  CBIASN PBIAS1 VCC    VCC PCH W=25U L=2.5U
MBP4  CNTR   CNTR   CBIASN VCC PCH W=25U        M=2
*
R1    PBIAS1 PBIAS2 4.55K
R2    PBIAS2 CNTR   1.84K
R3    CNTR   NBIAS2 1.84K
R4    NBIAS2 NBIAS1 4.55K
.DCVOLT CNTR=1.6 NBIAS1=0.9 PBIAS1=2.3 CBIASN=2.6 CBIASP=0.8
**********************************************************************
**  SUM Control transistors N1 and P1
**********************************************************************
MN1   VCC    CBIASN SUM    VSS NCH W=10U
MP1   VSS    CBIASP SUM    VCC PCH W=25U
**********************************************************************
.END
```



After the BIAS cell is designed, the sizing of the CBIAS network can be checked by this simulation. The voltage on SUM is swept through Vcc/2 and the currents through CN1 and CP1 are checked to be sure that they do not overlap by much. In this design, the strength of the clamp circuit (current at CNTR ± 300 mv) was increased to lower the gain of the buffer and make the design more stable.

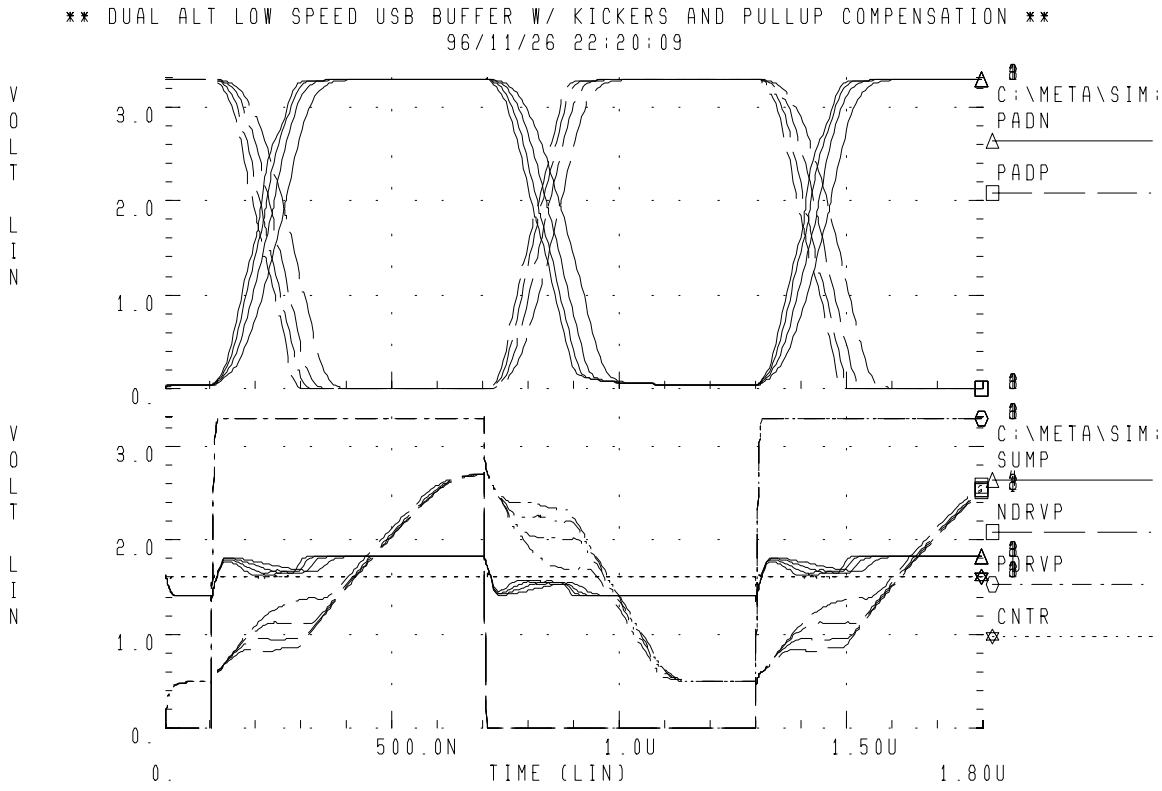
Full Buffer Simulations, Including Enhancements

```
** Dual Alt Low Speed USB buffer w/ kickers and pull-up compensation *
*********************************************************************
.LIB 'std08u.lib' EE
*********************************************************************
.TRAN 1NS 1800NS SWEEP LDCAP POI 4 50PF 100PF 200PF 400PF
.TEMP 25
.OPTION DEFL=0.8U DEFAD=40U DEFAS=40U
.PRINT TRAN  VPADN=V(PADN)               VPADP=V(PADP)
+            VPDRVN=V(PDRVN)             VNDRVN=V(NDRVN)
+            VSUMN=V(SUMN)
+            ICAPN=I(XLSBUFN.C1)         IMN14N=I(MNI4)
+            IMN1N=I(XLSBUFN.MN1)        IMP1N=I(XLSBUFN.MP1)
*********************************************************************
VCC3   VCC   0  DC=3.3V
VGND   VSS   0  DC=0.0V
VDUM   DUMMY 0  DC=3.3V
.GLOBAL VCC VSS
$.PARAM LDCAP=100PF
VBENB  BENB  0  DC=0.0V
VNENNN NENBN 0  PULSE 0.0 3.3 100NS 2NS 2NS 600NS 1200NS
VPENN  PENN  0  PULSE 0.0 3.3 100NS 2NS 2NS 600NS 1200NS
VNENNP NENBP 0  PULSE 3.3 0.0 100NS 2NS 2NS 600NS 1200NS
VPENP  PENP  0  PULSE 3.3 0.0 100NS 2NS 2NS 600NS 1200NS
*********************************************************************
**  BIAS cell
*********************************************************************
MBN1  NBIAS1 NBIAS1 VSS    VSS NCH W=10U L=2.5U M=5
MBN2  NBIAS1 BENB   VSS    VSS NCH W=10U
MBN3  CBIASP NBIAS1 VSS    VSS NCH W=10U L=2.5U
MBN4  CNTR   CNTR   CBIASP VSS NCH W=10U        M=2
*
MBP1  BND1   PBIAS1 VCC    VCC PCH W=25U L=2.5U M=5
MBP2  PBIAS1 BENB   BND1   VCC PCH W=25U        M=2
MBP3  CBIASN PBIAS1 VCC    VCC PCH W=25U L=2.5U
MBP4  CNTR   CNTR   CBIASN VCC PCH W=25U        M=2
*
R1    PBIAS1 PBIAS2 4.55K
R2    PBIAS2 CNTR   1.84K
R3    CNTR   NBIAS2 1.84K
R4    NBIAS2 NBIAS1 4.55K
.DCVOLT CNTR=1.6 NBIAS1=0.9 PBIAS1=2.3 CBIASN=2.6 CBIASP=0.8 NBD1=2.43
```

```
*********************************************************************
**  LSBUFF Cell
*********************************************************************
.SUBCKT LSBUFF NBIAS1 NBIAS2 PBIAS1 PBIAS2 CBIASN CBIASP CNTR PEN NENB
+       SUM NDRV NOFF PDRV PAD VDAT=3.3V VDATB=0.0V
*
**  SUM Clamp transistors NC and PC
*
MCN1  VCC    CBIASN SUM    VSS NCH W=10U
MCP1  VSS    CBIASP SUM    VCC PCH W=25U
*
** CURRENT SOURCE TO CAP WITH SWITCHES
*
MP1   SUM    PBIAS1 ND1    VCC PCH W=25U  L=2.5U      $ 'N' CAP CUR SRC
MP2   ND1    NENB   VCC    VCC PCH W=25U
MN1   SUM    NBIAS1 ND2    VSS NCH W=10U  L=2.5U      $ 'P' CAP CUR SRC
MN2   ND2    PEN    VSS    VSS NCH W=10U
*
** OP AMP DRIVING THE N OUTPUT DEVICE
*
MP5   TL1    PBIAS1 VCC    VCC PCH W=25U  L=2.5U M=2  $ TAIL CUR SRC
MP6   ND3    CNTR   TL1    VCC PCH W=25U  L=1.5U M=1  $ CNTR DIFF INP
MP7   ND4    SUM    TL1    VCC PCH W=25U  L=1.5U M=1  $ SUM  DIFF INP
MP8   VSS    NENB   ND4    VCC PCH W=25U              $ AMP SWITCH
MP9   NDRV   NENB   ND3    VCC PCH W=25U              $ AMP SWITCH
MP9A  NDRV   NOFF   ND3    VCC PCH W=25U              $ P-U COMP BYPASS
MN10  NDRV   NBIAS2 NCAS   VSS NCH W=10U              $ LOAD CASCODE
MN11  NCAS   NBIAS1 VSS    VSS NCH W=10U  L=2.5U      $ LOAD
*
** N-OUTPUT DEVICE, ENABLE AND KICKER
*
MN3   NDRV   NENB   ND7    VSS NCH W=10U
MN3A  ND7    NOFF   VSS    VSS NCH W=10U
MN4   PAD    NDRV   VSS    VSS NCH W=300U L=1.0U
MN4A  VSS    NDRV   VSS    VSS NCH W=450U L=1.0U
MN12  NKR    NBIAS2 NDRV   VSS NCH W=10U
MP13  NKR    NENB   VCC    VCC PCH W=25U
*
**************************************
*
** OP AMP DRIVING THE P OUTPUT DEVICE
*
MN5   TL2    NBIAS1 VSS    VSS NCH W=10U  L=2.5U M=2  $ TAIL CUR SRC
MN6   ND5    CNTR   TL2    VSS NCH W=10U  L=1.5U M=1  $ CNTR DIFF INP
MN7   ND6    SUM    TL2    VSS NCH W=10U  L=1.5U M=1  $ SUM  DIFF INP
MN8   VCC    PEN    ND6    VSS NCH W=10U              $ AMP SWITCH
MN9   PDRV   PEN    ND5    VSS NCH W=20U              $ AMP SWITCH
MP10  PDRV   PBIAS2 PCAS   VCC PCH W=25U              $ LOAD CASCODE
MP11  PCAS   PBIAS1 VCC    VCC PCH W=25U  L=2.5U      $ LOAD
*
** P-OUTPUT DEVICE, ENABLE AND KICKER
*
MP3   PDRV   PEN    VCC    VCC PCH W=10U
MP4   PAD    PDRV   VCC    VCC PCH W=750U L=1.0U
MP12  PKR    PBIAS2 PDRV   VCC PCH W=25U
MN13  PKR    PEN    VSS    VSS NCH W=10U
*
C1    PAD    SUM    1PF
*
.DCVOLT PAD=VDAT SUM=1.6   NDRV=VDATB PDRV=VDATB ND1=VDAT  ND2=VDATB
+       ND3=VDAT ND4=VDAT  ND5=VDATB  ND6=VDATB  PCAS=VDAT NCAS=VDATB
+       TL1=VDAT TL2=VDATB NKR=1.6    PKR=1.6    NOFF=VDATB
*
```

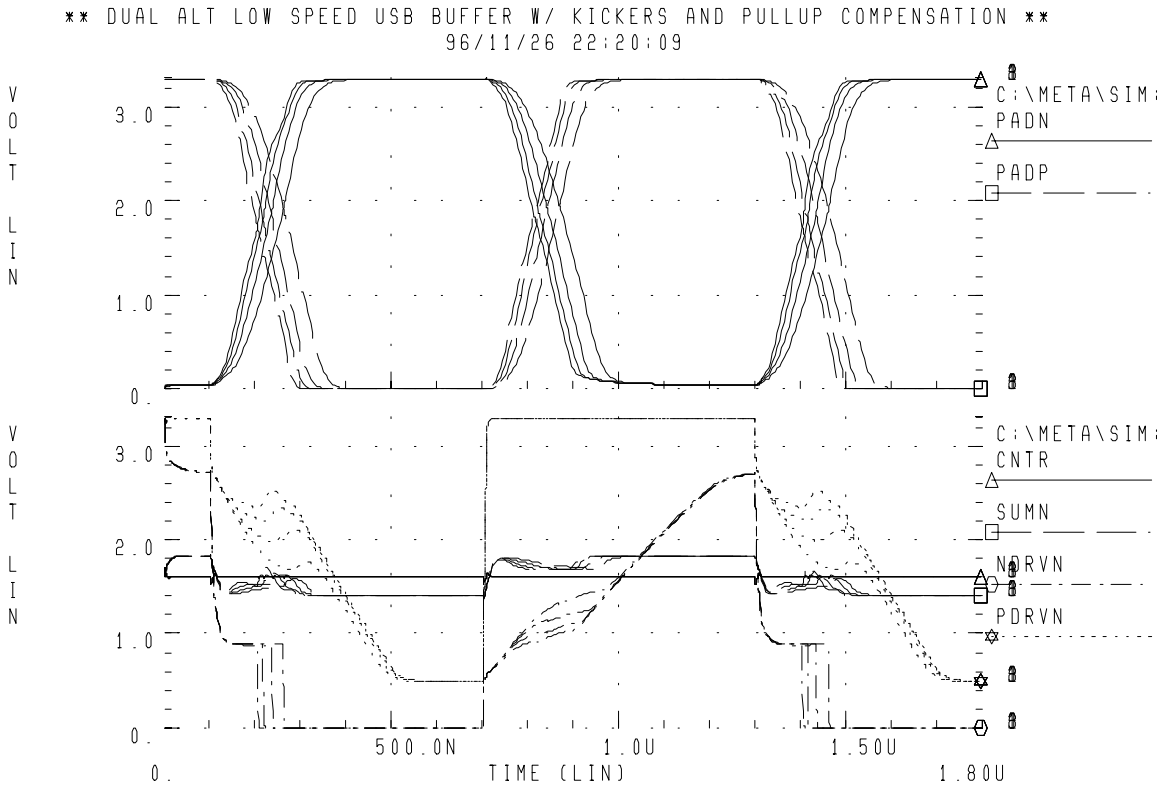
```
CLDP  PAD  VSS    LDCAP
RPDP  PAD  VSS    15K
*
.ENDS
********************************************************************
**  Subcell Usage
********************************************************************
*
**  PAD-P:   ( PAD-P STARTS OUT HIGH )
*
XLSBUFP NBIAS1 NBIAS2 PBIAS1 PBIAS2 CBIASN CBIASP CNTR PENP NENBP SUMP
+       NDRVP DUMMY PDRVP PADP LSBUFF VDAT=3.3V VDATB=0.0V
*
**  PAD-N:   ( PAD-P STARTS OUT LOW  )
*
XLSBUFN NBIAS1 NBIAS2 PBIAS1 PBIAS2 CBIASN CBIASP CNTR PENN NENBN SUMN
+       NDRVN DIFF PDRVN PADN LSBUFF VDAT=0.0V VDATB=3.3V
*
MN14  CM1    NDRVN  CM2    VSS NCH W=10U  L=1.0U      $ PULL-UP COMP
MN14A CM2    NDRVN  VSS    VSS NCH W=10U  L=1.0U
MN15  NDRVN  NENBN  CM1    VSS NCH W=10U
EDIFF DIFF   VSS    PADN  PADP 1000 MAX=3.3V MIN=0.0V $ DIFF INPUT BUFF
.DCVOLT CM1=0.0 CM2=0.0
*
RPUN  VCC    PADN   1.5K

********************************************************************
** PREDRV Cell is being behaviorally simulated by driving NENB and PEN
********************************************************************
.END
```



This simulation shows the final design, including the performance improvements for buffer turn-on delay ("kickers") and compensation for the USB pull-up resistor. The top curves are the buffer outputs. The family of four curves represent the outputs for capacitive loads between 50 pF and 400 pF. The output slope is very constant across the 8:1 range of load. There is about 20ns of skew between J-to-K state transitions and K-to-J state transitions which is within spec.

The bottom set of curves are key signals in the D+ output predriver. SUMP is the SUM node in the positive (D+) driver. When the buffer is going to switch states, the sign of SUM changes. The buffer tries to hold SUM close to CNTR while the buffer is switching. After that, SUM goes as far as the clamp circuit allows. The NDRVP and PDRVP signals are the output transistor gate voltages. The effects of the kickers can be seen as these signals jump to about 0.5 volts from the rail before charging to the level needed to sustain the desired output edge rate. The gate voltage remains relatively flat during the transition. After the output swing is done, the gates charge to about 0.5 volts of the rail to establish full drive on the output transistor.



This set of curves shows the signals for the D- driver, including the pull-up compensation. The output pad signals are included for reference. The SUM node signal is inverted for SUMN in the D- driver from the D+ driver above, but otherwise the same. The same is generally true for the output transistor gate drive nodes (NDRVN and PDRVN), with two exceptions. Of note is the voltage on NDRV during the first part of the positive transition of the D- line. NDRV is held at about 0.8 volts to cause N4 to sink about 1.0 mA of current to counteract the effects of the USB pull-up. It goes to ground as soon as the D- and D+ lines cross. PDRV is not as flat during the transition as in the D+ buffer above. The gate drive on the P-channel pull-up transistor has to change to compensate for the loss of load current that occurs when the pull-up resistor compensation current is switched off.